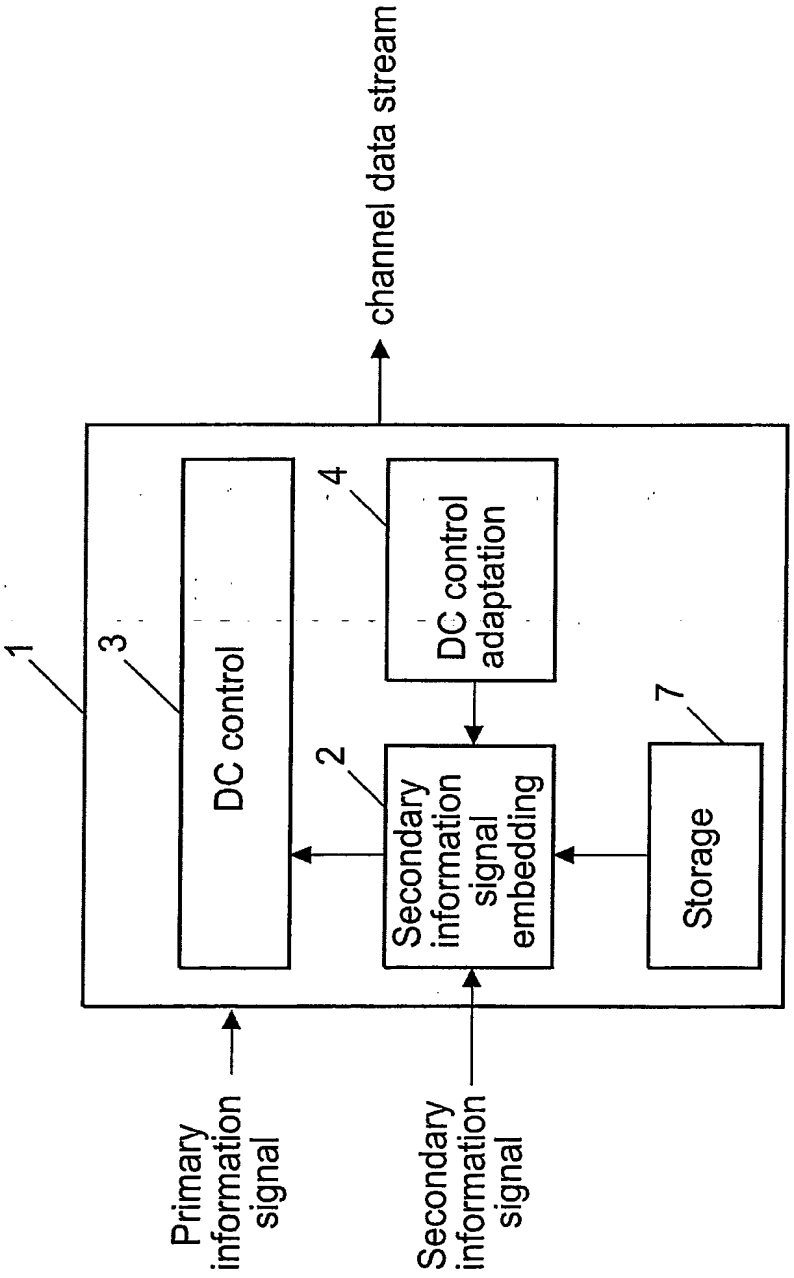

channel data stream
1
3
DC control
4
DC control adaptation
2
Secondary information signal embedding
7
Storage
Primary information signal
Secondary information signal

Fig.1

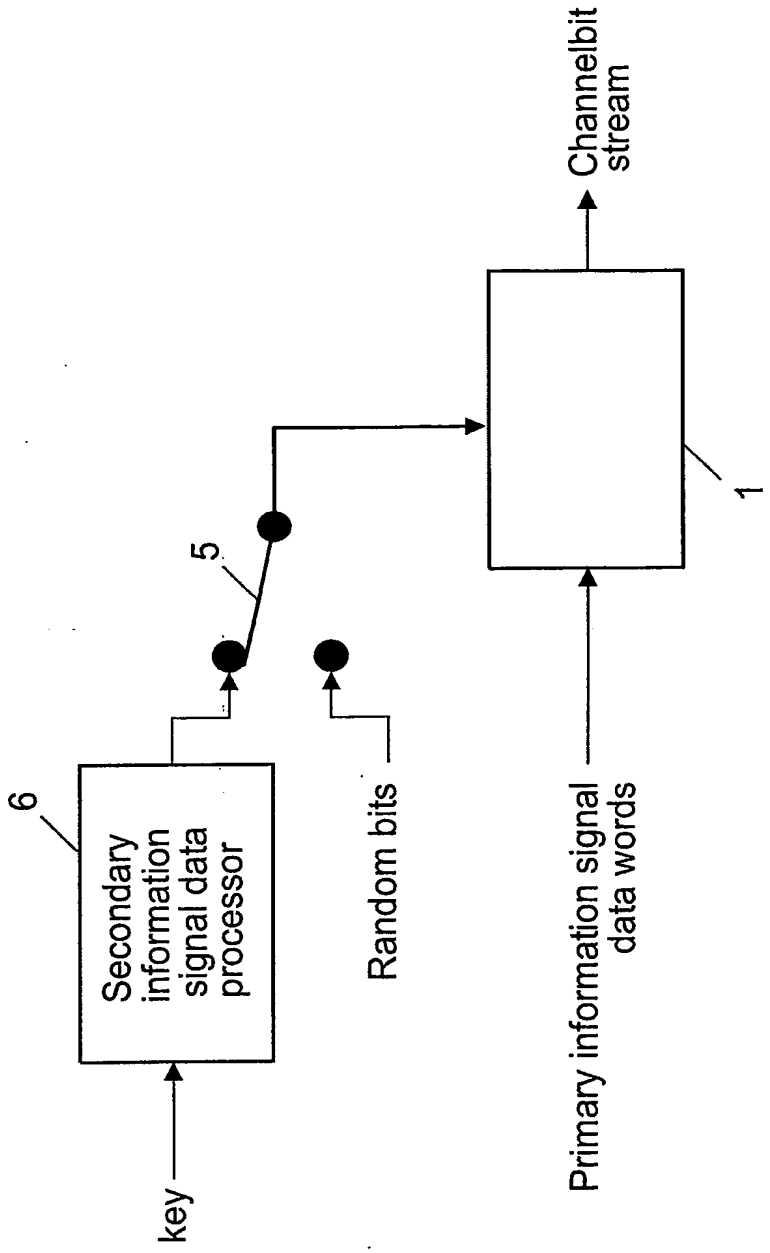

Channelbit stream
1
5
6
Secondary information signal data processor
Random bits
Primary information signal data words
key

Fig.2

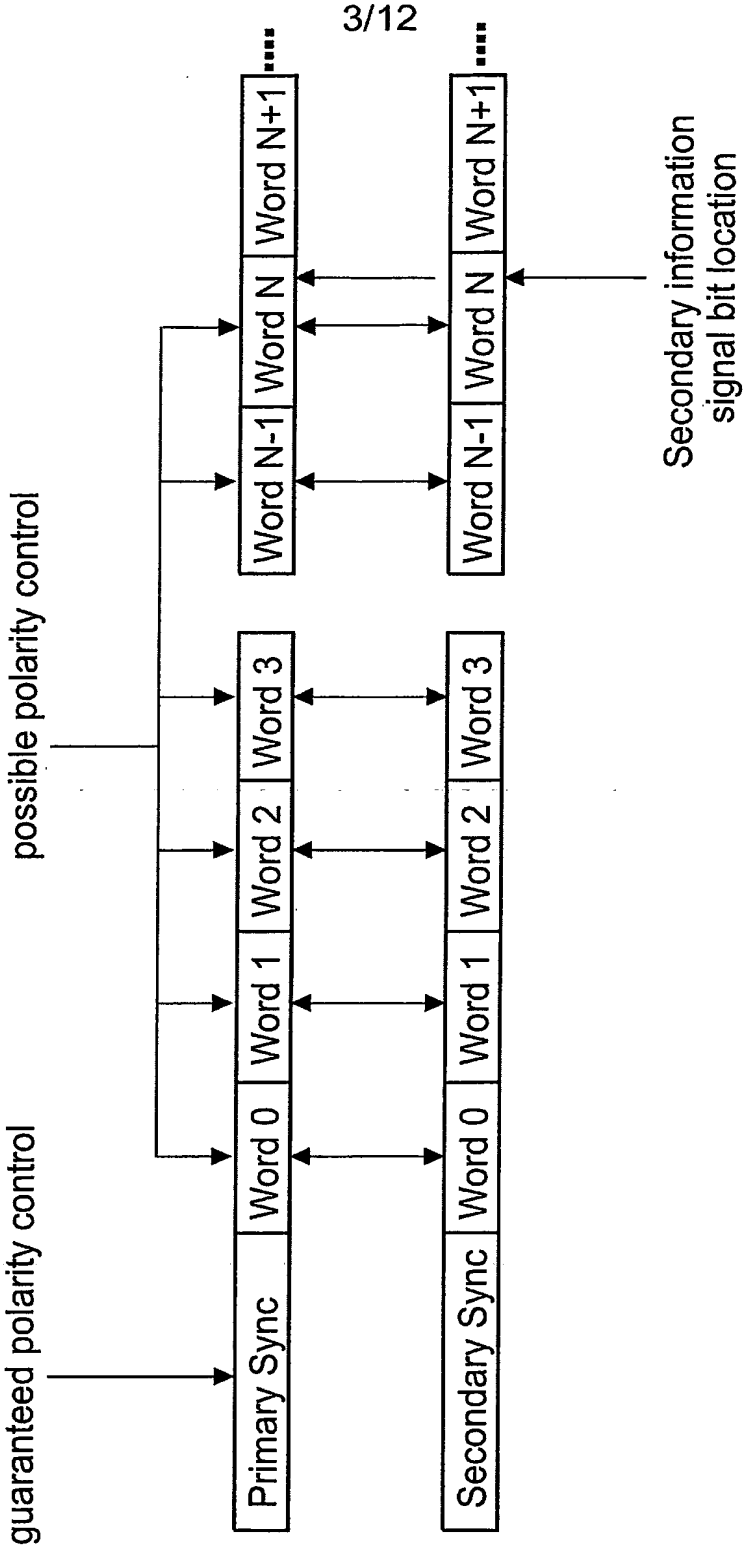

guaranteed polarity control
possible polarity control
Secondary information signal bit location
Primary Sync
Word 0
Word 1
Word 2
Word 3
Word N-1
Word N
Word N+1
Secondary Sync
Word 0
Word 1
Word 2
Word 3
Word N-1
Word N
Word N+1

Fig.3

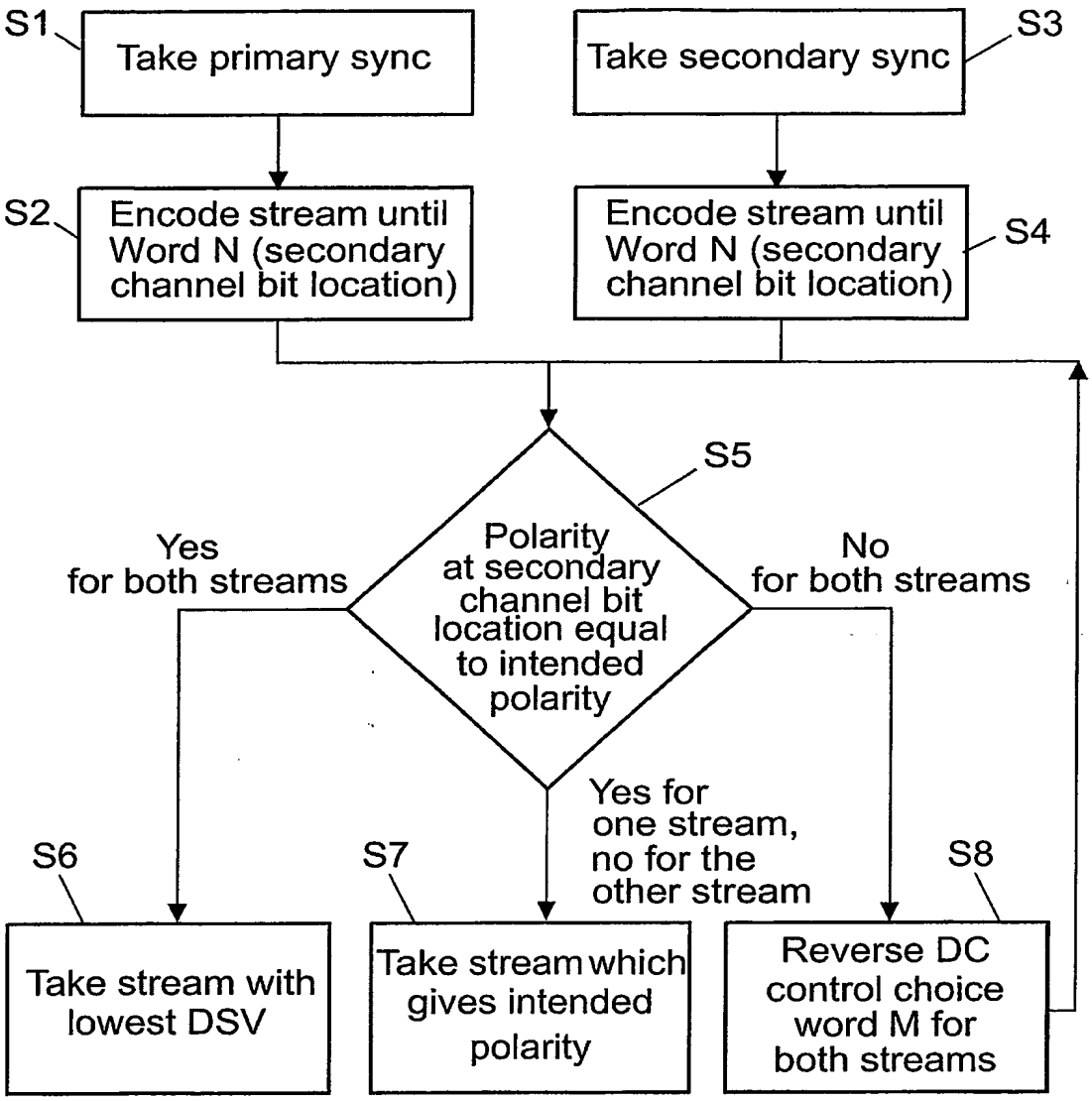

S1
Take primary sync
S3
Take secondary sync
S2
Encode stream until Word N (secondary channel bit location)
S4
Encode stream until Word N (secondary channel bit location)
S5
Polarity at secondary channel bit location equal to intended polarity
Yes for both streams
No for both streams
Yes for one stream, no for the other stream
S6
Take stream with lowest DSV
S7
Take stream which gives intended polarity
S8
Reverse DC control choice word M for both streams

Fig.4

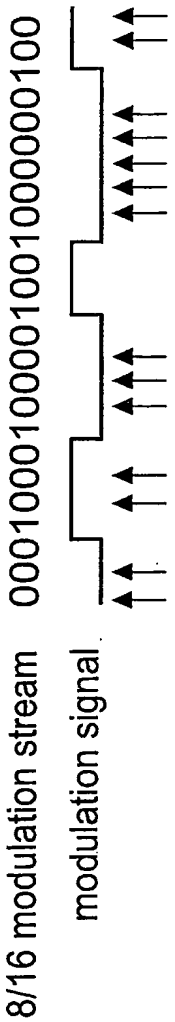
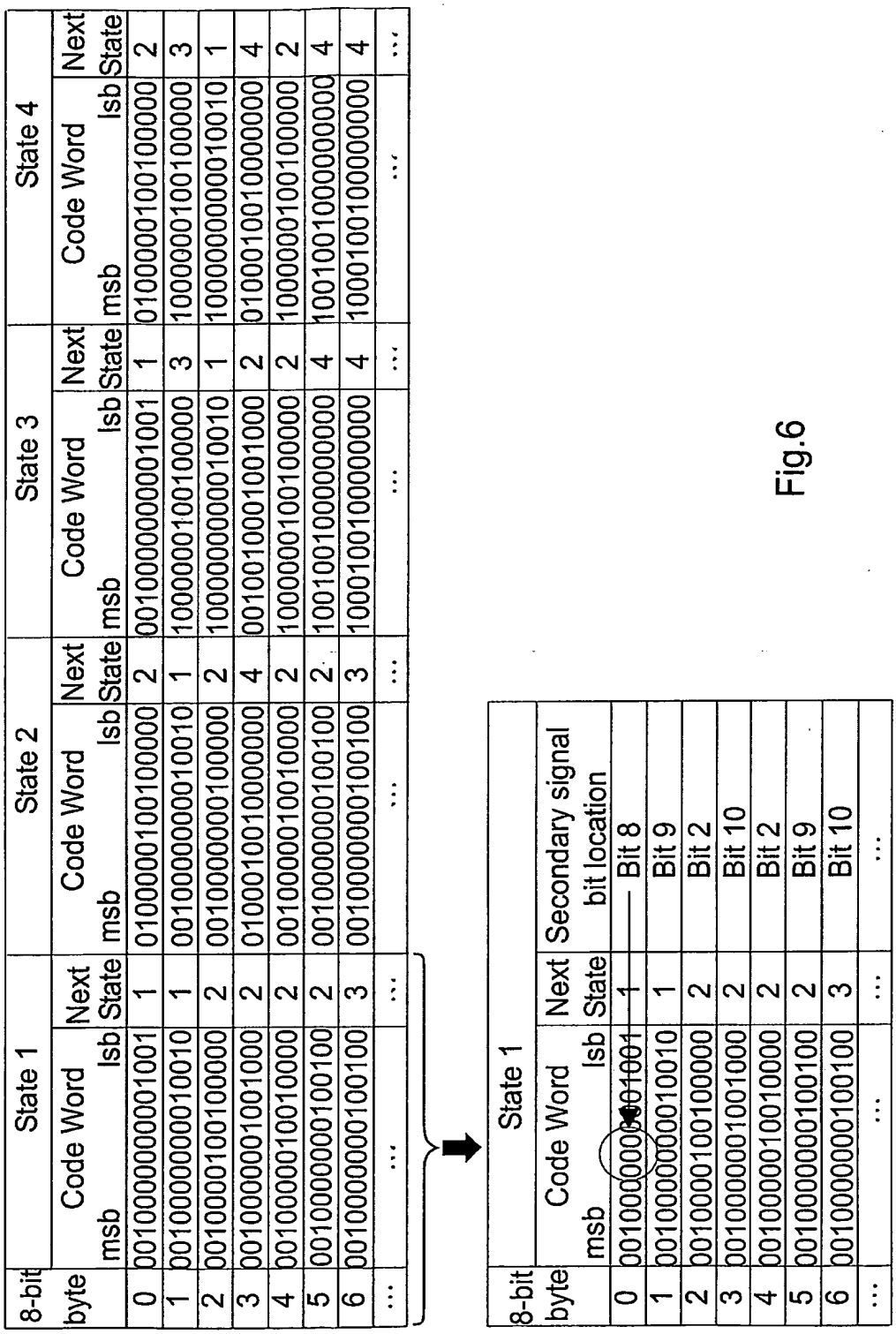

8/16 modulation stream
modulation signal
000100010000100100000100

Fig.5



8-bit byte	State 1		State 2		State 3		State 4	
	Code Word msb lsb	Next State	Code Word msb lsb	Next State	Code Word msb lsb	Next State	Code Word msb lsb	Next State
0	0010000000001001	1	0100000100100000	2	0010000000001001	1	0100000100100000	2
1	0010000000010010	1	0010000000010010	1	1000000100100000	3	1000000100100000	3
2	0010000100100000	2	0010000000100000	2	1000000000010010	1	1000000000010010	1
3	0010000001001000	2	0100010010000000	4	0010010001001000	2	0100010010000000	4
4	0010000010010000	2	0010000010010000	2	1000000100100000	2	1000000100100000	2
5	0010000000100100	2	0010000000100100	2	1001001000000000	4	1001001000000000	4
6	0010000000100100	3	0010000000100100	3	1000100100000000	4	1000100100000000	4
...	...	...	...	...	...	...	...	...

8-bit byte	State 1		
	Code Word msb lsb	Next State	Secondary signal bit location
0	0010000000001001	1	Bit 8
1	0010000000010010	1	Bit 9
2	0010000100100000	2	Bit 2
3	0010000001001000	2	Bit 10
4	0010000010010000	2	Bit 2
5	0010000000100100	2	Bit 9
6	0010000000100100	3	Bit 10
...	...	...	...

Fig.6

Sync frame	Code word
0	2
1	88
2	6
...	...

Fig.7a

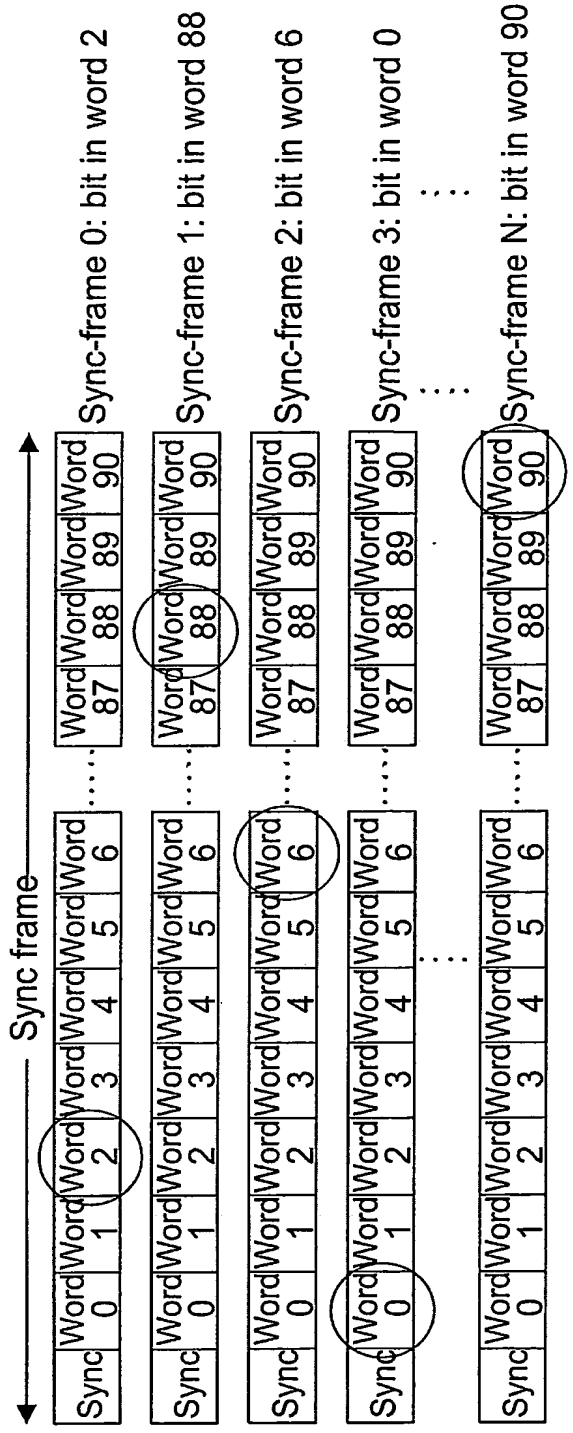


Fig.7b

Rec frame	Code word
0	2
1	3
2	0
...	...

Fig.8a

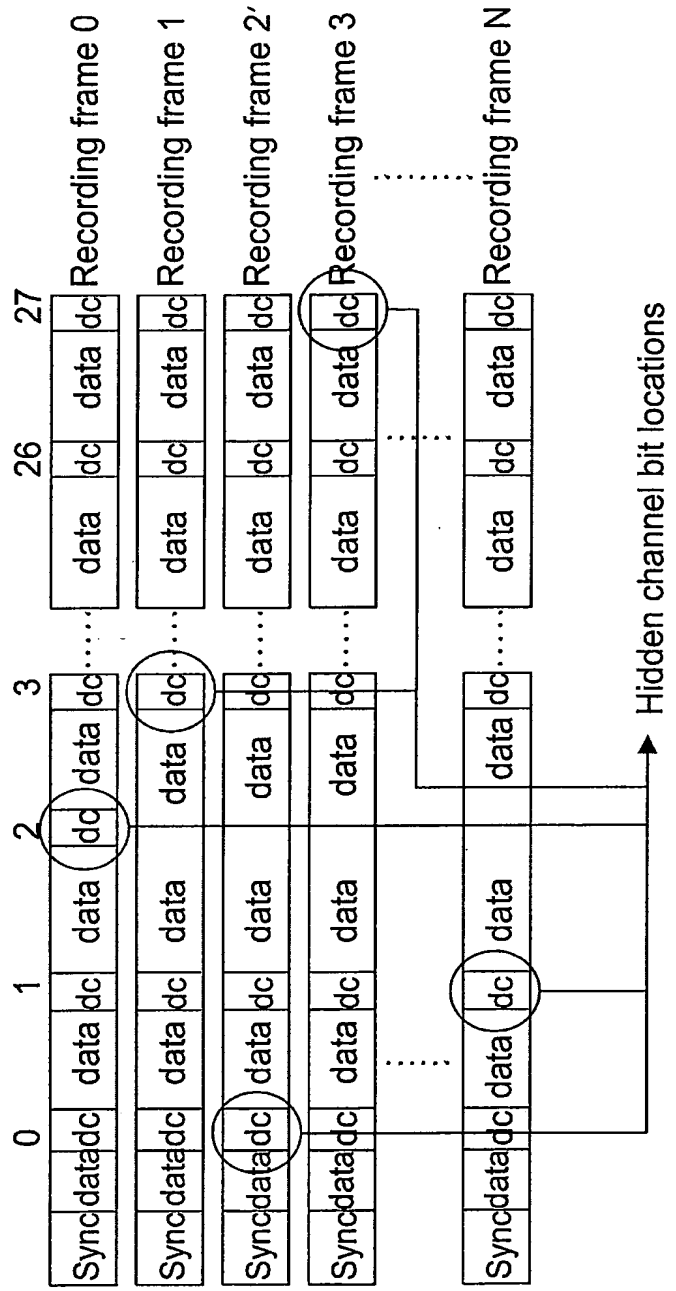


Fig.8b

Subcode frame	Code word
0	Word 2
1	Merging bit pattern 1
2	Merging bit pattern 31
...	...

Fig.9a

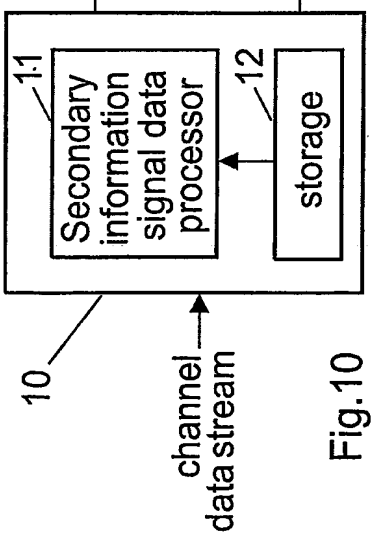


Fig.10

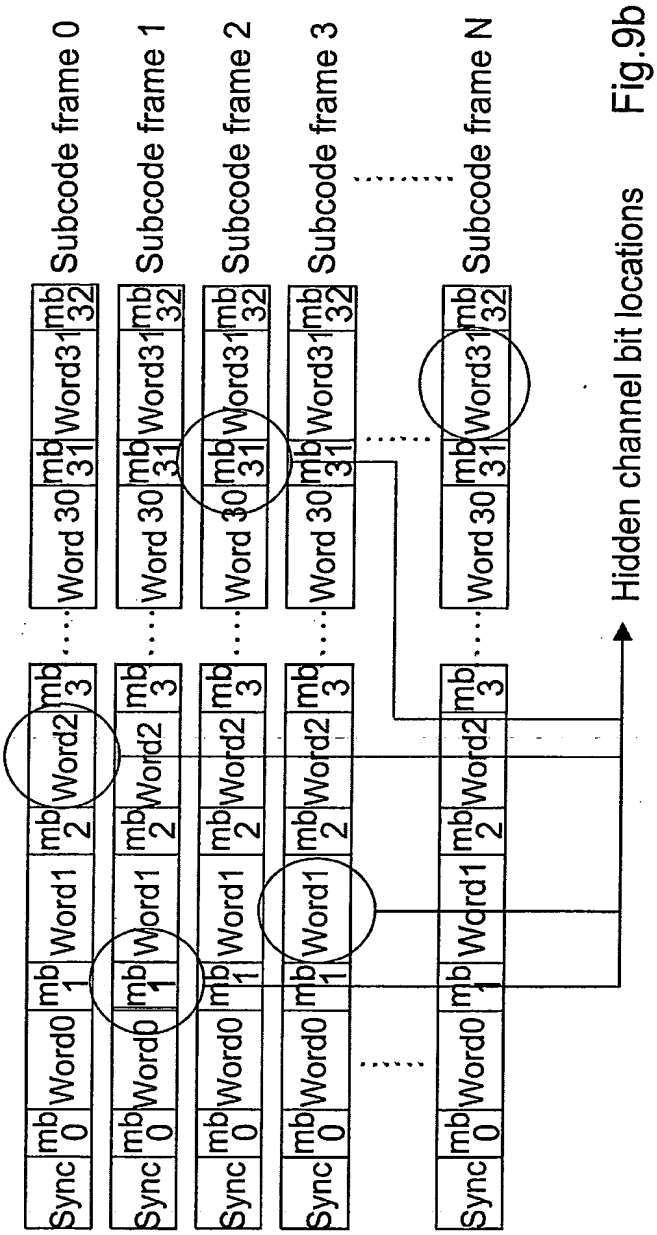


Fig.9b

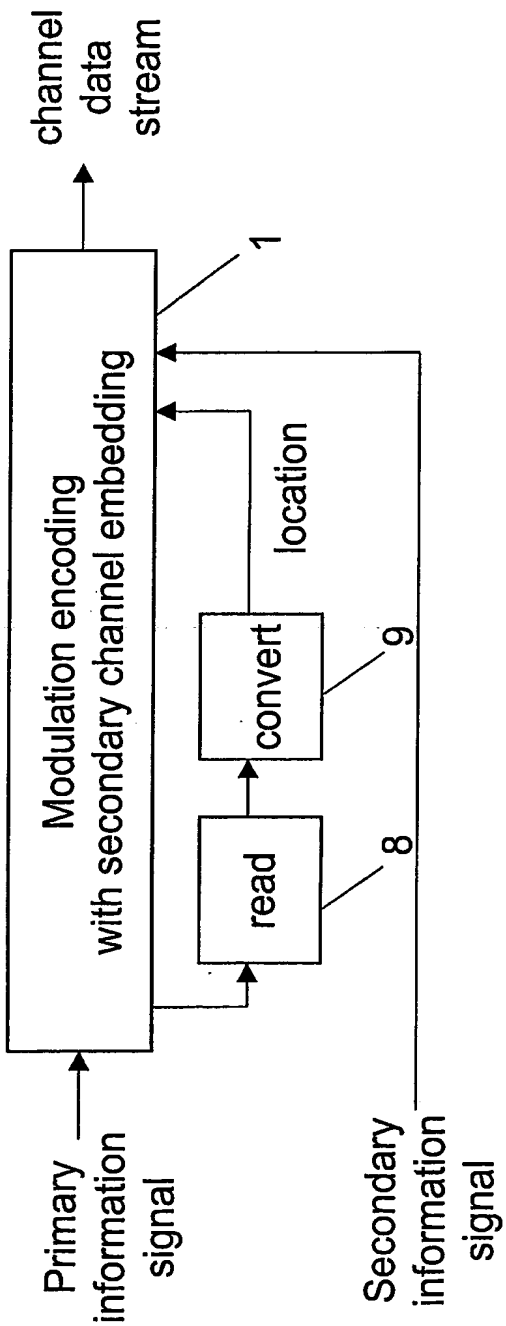

channel data stream
1
Modulation encoding with secondary channel embedding
location
convert
9
read
8
Primary information signal
Secondary information signal

Fig.11

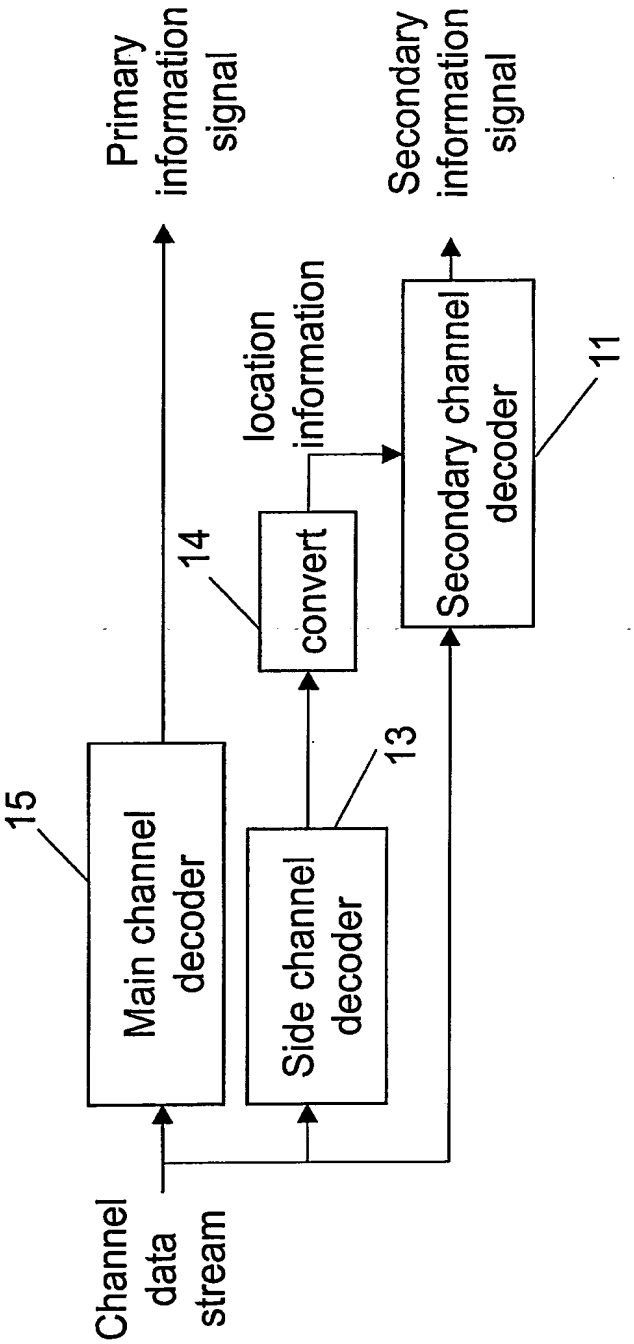

Primary information signal
Secondary information signal
location information
Secondary channel decoder
11
14
convert
13
15
Main channel decoder
Side channel decoder
Channel data stream

Fig.12

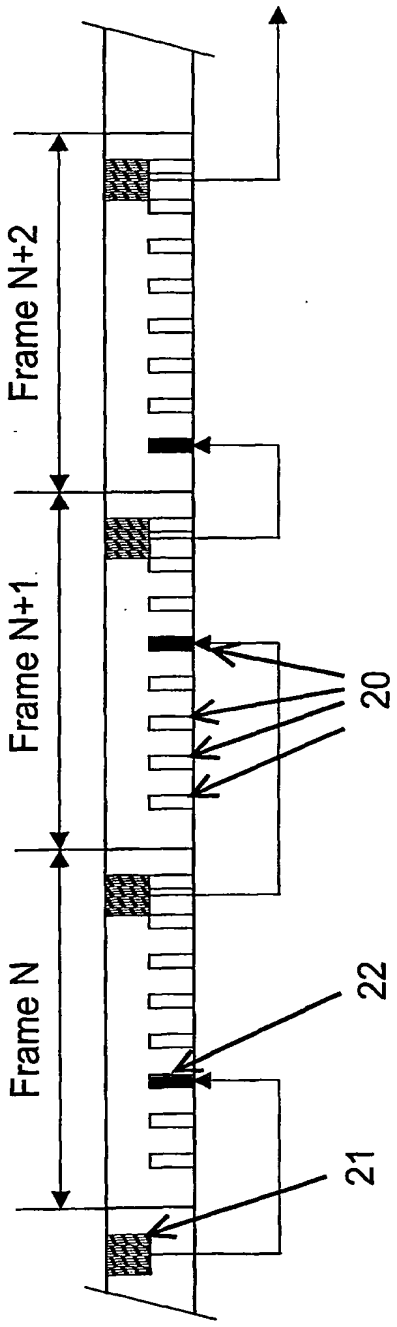


Fig.13